REMARKS

Claims 1 -2, 5 – 6, 9 – 10, 12, 14 – 19, and 23 - 29 are pending. Claims 9 and 23 – 26 have been amended. Claims 27 – 29 have been added. No new matter has been introduced. Reexamination and reconsideration of the present application are respectfully requested.

In the Final Office Action dated July 8, 2003, the Examiner objected to the drawings under 37 CFR 1.83(a). The Examiner rejected claims 23 – 26 under 35 U.S.C. § 112, second paragraph, as being indefinite. The Examiner rejected claims 1, 5, 23 – 26 as being unpatentable over U.S. Patent No. 6,281,527 to Chen (the Chen reference) in view of Applicant Admitted Prior Art. The Examiner rejected claims 5 and 25 – 26 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,570,226 to Groeseneken (the Groeseneken reference) in view of Applicant Admitted Prior Art. The Examiner rejected claims 2 and 6 under 35 U.S.C. § 103(a) as being unpatentable over Chen and AAPA, and further in view of U.S. Patent No. 5,477,413 to Watt (the Watt reference). The Examiner rejected claim 6 under 35 U.S.C. § 103(a) as being unpatentable over the Groeseneken reference and AAPA and further in view of the Watt reference. The Examiner rejected claims 9 and 15 – 18 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 3,955,210 to Bhatia (the Bhatia reference). The Examiner rejected claims 10, 12, and 19 under 35 U.S.C. § 103(a) as being unpatentable over Bhatia in view of AAPA. The Examiner rejected claim 14 under 35 U.S.C. § 103(a) as being unpatentable over the Bhatia reference in view of the Iwase reference, and further in view of the Watt reference. Applicants respectfully traverse these rejections.

In a telephonic interview dated January 5, 2004, with Examiner Nadev, Examiner Nadev agreed to withdraw the objection to the drawings.

In the telephonic interview dated January 5, 2004, with Examiner Nadev, both parties agreed to identify that the voltage applied to the input terminal should be described by utilizing the terms "positive bias" or "negative bias" rather than the phrase "voltage of a first polarity" in claims 23 – 26. Applicants have amended claims 23 – 26 to utilize the terms positive bias or negative bias. Therefore, the Examiner's 35 U.S.C. § 112, second paragraph rejection has been overcome.

The present invention is directed to an input protection circuit for an integrated circuit device. The input protection circuit protects the circuit from electrostatic discharge (ESD). A lateral PNP transistor PB and a lateral NPN transistor NB are serially connected between an input terminal and a reference potential. Within the transistor PB, a PN junction diode D1 is formed. In the transistor NB, a PN junction diode D3 is formed. If a positive bias large ESD voltage is input, the transistor NB turns on. If a negative bias large ESD voltage is input, the transistor PB turns on.

Independent claim 1, as amended, recites:

An input protection circuit comprising:

an input terminal for supplying an input signal to a circuit to be protected;

a semiconductor substrate of a first conductivity type;

a first well region of a second conductivity type opposite to the first conductivity type, said first well region being formed in one principal surface area of said semiconductor substrate and forming a PN junction with said semiconductor substrate;

first and second impurity doped regions of the first conductivity type formed in said first well region and forming a first lateral bipolar transistor with a portion of said first well region serving as a base;

a second well region of the first conductivity type formed in the principal surface area of said semiconductor substrate;

third and fourth well regions of the second conductivity type formed in said second well region and forming a second lateral bipolar transistor with a portion of said second well region serving as a base, bottoms

of said third and fourth well regions forming a PN junction with said second well or with said semiconductor substrate; and a circuit formed in said semiconductor substrate and connected to said input terminal;

wherein said input terminal is connected to said first impurity doped region, said second impurity doped region and the base of said first lateral bipolar transistor are connected to said third well region, said first lateral bipolar transistor operating without a fixed base bias, and said fourth well region and the base of the second lateral bipolar transistor are connected to one reference potential node.

The Chen reference is directed to an ESD protection circuit for protecting a circuit, comprising a lateral semiconductor-controlled rectifier, a MOS transistor, and a current-sinking device. The Chen reference includes a p-type doped region 32 and an N-type doped region 33 that are spaced apart and formed in a N-type semiconductor layer 31, wherein the P-type doped region 32 is closer to the junction 40 than the N-type doped region 33. Another N-type doped region 34 and P-type doped region 35 are spaced apart and formed in the P-type semiconductor layer 30, wherein the N-type doped region 34 is closer to the junction 40 than the P-type doped region 33. The P-type doped region 33 and the N-type doped region 32 are connected together to the IC pad , which is coupled to the internal circuit 2 to be protected by the ESD protection circuit. The N-type doped region 34 and the P-type doped region 35 are connected together to the power node Vss, that is at ground potential. *(Chen, Col. 3, lines 1 - 26)*.

In addition, an N-type doped region 36 is provided with one portion formed in the N--type semiconductor layer 31 and another portion formed in the P-type semiconductor layer 30 so as to span the junction 40 therebetween. A gate structure 37 overlies a portion of the P-type semiconductor 30 between the N-type doped regions 34 and 36, comprising, from bottom to top, an oxide layer 38 and an electrode layer 39. The oxide layer 38 is formed on the P-type semiconductor layer 30 where the electrode layer 39 is connected to the node Vss. Accordingly, the P-type doped region 32, N-type

semiconductor layer 31, and P-typed doped region 41 constitute the emitter, base, and collector of a first PNP bipolar junction transistor 42A. The P-type semiconductor layer 32, N-type semiconductor layer 31, and P-type semiconductor layer 30 constitute the emitter base, and collector of a second PNP bipolar junction transistor 42B. The P-type semiconductor layer 30, N-type semiconductor layer 31, and N-typed doped region 34 constitute the collector, base, and emitter of an NPN bipolar junction transistor. *(Chen, Col. 3, lines 28 - 55).*

The Chen reference does not disclose, teach, or suggest the input protection circuit of claim 1, as amended. The Chen reference does not concern an input protection circuit including an input terminal for supplying an input signal to a circuit to be protected; a semiconductor substrate of a first conductivity type; a first well region of a second conductivity type opposite to the first conductivity type, said first well region being formed in one principal surface area of said semiconductor substrate and forming a PN junction with said semiconductor substrate; first and second impurity doped regions of the first conductivity type formed in said first well region and forming a first lateral bipolar transistor with a portion of said first well region serving as a base; a second well region of the first conductivity type formed in the principal surface area of said semiconductor substrate; ***third and fourth well regions of the second conductivity type formed in said second well region and forming a second lateral bipolar transistor with a portion of said second well region serving as a base***, bottoms of said third and fourth well regions forming a PN junction with said second well or with said semiconductor substrate; and a circuit formed in said semiconductor substrate and connected to said input terminal; wherein said input terminal is connected to said first impurity doped region, said second

impurity doped region and the base of said first lateral bipolar transistor are connected to said third well region, said first lateral bipolar transistor operating without a fixed base bias, and said fourth well region and the base of the second lateral bipolar transistor are connected to one reference potential node.

The Examiner states that the third and fourth regions 36 and 34 of the second conductivity type formed in the second well region form a second lateral bipolar transistor with a portion of the second well region serving as a base. *(July 8 Office Action, page 4)*. The Chen reference discloses three bipolar junction transistors: 1) P-type dope region 32, N-type semiconductor layer 31, and P-type doped region 41 constituting the emitter, base, and collector of a first bipolar junction transistor 42A; 2) P-type semiconductor layer 32, N-type semiconductor layer 32, N-type semiconductor layer 31, and P-type semiconductor layer 30 constitute the emitter, base, and collector of a second bipolar junction transistor 42; and 3) P-type semiconductor layer 30, N-type semiconductor layer 31, and N-typed doped region 34 constitute the collector, base, and emitter of an NPN bipolar junction transistor. This is not the same as an input protection circuit including ***third and fourth well regions of the second conductivity type formed in said second well region and forming a second lateral bipolar transistor with a portion of said second well region serving as a base.*** It is not the same because the Chen reference's third and fourth regions 34 and 36 are not disclosed as forming a second lateral bipolar transistor. Accordingly, applicants respectfully submit that independent claim 1 distinguishes over the Chen reference.

Independent claim 1 further distinguishes over the Chen reference. The Chen reference does not disclose, teach, or suggest the input protection circuit of claim 1. The

Chen reference does not disclose a input protection circuit wherein **said second impurity doped region and the base of said first lat ral bipolar transistor are connected to said third well region**. Instead, the Chen reference discloses that the second well region 41 is coupled to Vss (ground potential) and the base 31 of the first lateral bipolar transistor is connected to the third region 36. The Chen reference does not disclose that the second impurity doped region is connected to the third well region 36. Accordingly, applicants respectfully submit that independent claim 1 further distinguishes over the Chen reference.

The Examiner indicated that Fig. 10 of the present invention is applicant admitted prior art (AAPA). The Examiner states that the AAPA in figure 10 teaches third and fourth regions 5 and 6 being formed in third and fourth well regions 3 and 4. *(July 8 Office Action, page 4)*. The AAPA discloses an input protection circuit including a MOS transistor which is formed by N-type well region 2. The bottoms of n-type well regions 3 and 4 form PN junctions with the substrate 1. In the well regions 3 and 4, n-type impurity doped regions 5 and 6 are formed to provide contact regions, and in the p-type well region 2, a p-type impurity doped region 7 is formed to provide a contact region. The impurity doped region 5 and the gate electrode layer 9 are connected to an input terminal. The impurity doped regions 6 and 7 are connected to ground potential. *(Specification, Fig. 10 and pages 1 and 2)*.

The AAPA does not disclose, teach, or suggest, the input protection circuit of claim 1. The AAPA does not concern an input protection circuit including ***third and fourth well regions of the second conductivity type formed in said second well region and forming a second lateral bipolar transistor with a portion of said second well region serving as a base.*** The AAPA only discloses first and second well regions 3 and 4 formed

in a p-well 2, and forming a transistor BT. There is not disclosure of third and fourth well regions nor is there disclosure of a second lateral bipolar transistor being formed. Accordingly, applicants respectfully submit that independent claim 1 distinguishes over the AAPA, alone or in combination with the Chen reference.

Independent claim 1 further distinguishes over the AAPA. The AAPA does not teach, suggest, or disclose the input protection circuit of claim 1. The AAPA does not concern an input protection circuit wherein **said second impurity doped region and the base of said first lateral bipolar transistor are connected to said third well region**. Because there is no third well region in the AAPA, it would be impossible for the second impurity dope region and the base of said first lateral bipolar transistor are connected to said third well region. Accordingly, applicants respectfully submit that independent claim 1 distinguishes over the AAPA, alone or in combination with the Chen reference.

The Watt reference does not make up for the deficiencies of the Chen reference and the AAPA. The Examiner states that the Watt reference teaches forming a resistor in on a semiconductor substrate. *(July 8 Office Action, page 8)*. Assuming, arguendo, that the Watt reference does disclose the forming of a resistor on a semiconductor substrate, the Watt reference does not disclose an input protection circuit including ***third and fourth well regions of the second conductivity type formed in said second well region and forming a second lateral bipolar transistor with a portion of said second well region serving as a base*** or an input protection circuit wherein **said second impurity doped region and the base of said first lateral bipolar transistor are connected to said third well region.** Accordingly, applicants respectfully submit that claim 1 distinguishes over the Watt reference, alone or in combination with the Chen reference and the AAPA.

Further, applicants respectfully submit that the Chen reference and the AAPA cannot be combined because there is no teaching, suggestion, or incentive to support the combination of the Chen reference and the AAPA. The Chen reference does not disclose that its third and fourth regions (36 and 34) can be well regions, as supported by the Examiner's statement "Chen does not teach third or fourth regions being third and fourth well regions." *(July 8, 2003 Office Action, page 4).* The AAPA does not mention or disclose a circuit including the use of third and fourth regions being well regions and forming a second lateral bipolar transistor. By combining these references, the Examiner has impermissibly used "hindsight" by using the applicant's teaching as a blueprint to hunt through the prior art for the claimed elements and then combine them as claimed. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991).

In addition, the combination of the Chen reference with the AAPA reference would destroy the purpose and intent of the invention disclosed in the Chen reference. This would be a disincentive for combining the references. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984). The AAPA discloses an n-channel MOS transistor FT which includes a drain (well region 3), a gate (electrode layer 9), and a source (well region 4). The AAPA also discloses a bipolar transistor BT made of well regions 3 and 4 and a p-type region (portion of the well region 2). Placing the AAPA's circuit into the Chen reference would destroy the purpose of the Chen reference because of the different electrical connections to the drain, gate, and source of the MOS transistor that are present in the AAPA.

Claims 2, 23, 24, and 27 - 29 depend, directly or indirectly, on claim 1, as amended. Accordingly, applicants respectfully submit that claims 2, 23, 24, and 27 - 29

distinguish over the Chen and Watt references and the AAPA, alone or in combination.

Claim 27 further distinguishes over the Chen reference and the Applicant Admitted Prior Art. Claim 27 recites:

> The input protection circuit of claim 1, wherein the third well region is formed entirely inside the second well region.

The Chen reference does not disclose, teach, or suggest the input protection circuit of claim 27. The third well region 36 of the Chen reference is provided with one portion formed in the N-type semiconductor layer 31 and another portion formed in the P-type semiconductor layer 30 so as to span the junction therebetween. *(Chen, Col. 3, lines 27 - 31)*. Thus, the third well region of the Chen reference is not formed entirely inside the second well region, as recited in claim 27. Accordingly, applicants respectfully submit that claim 27 further distinguishes over the Chen reference.

Claim 27 further distinguishes over the AAPA, alone or in combination with the Chen reference. The AAPA teaches two n-type well regions 3 and 4, and a p-type well region (portion of well region 2) forming a lateral bipolar transistor, but does not teach that a third well region, which is part of a second lateral bipolar transistor, that is formed entirely inside the second well region. Accordingly, applicants respectfully submit that claim 27 further distinguishes over the AAPA, alone or in combination with the Chen reference.

Claim 28 further distinguishes over the Chen and AAPA references. Claim 28 recites:

> The input protection circuit of claim 1, wherein the third and fourth well regions have a depth almost equal to the second well region.

The Chen reference does not disclose, teach, or suggest the input protection circuit of claim 28. In the Chen reference, the third and fourth well regions cited by the Examiner, i.e., well regions 36 and 34, are not shown to have the depth of the p-well 40. *(Chen, Fig. 3)*. The depth of the well regions 36 and 34 in the Chen reference is less than half the depth of the p-well 40. This is not the same as third and fourth well regions having a depth almost equal to the second well region. Accordingly, applicants respectfully submit that claim 28 further distinguishes over the Chen reference.

AAPA does not make up for the deficiencies of the Chen reference. AAPA discloses N-type well regions 3 and 4 in a p-well region 2, but these well regions do not form a second lateral bipolar transistor for the circuit, the Chen's well regions only form a first bipolar transistor. Thus, the AAPA has no third and fourth well regions as recited in claim 28. Therefore, it would be impossible for the third and fourth well regions to have a depth almost equal to the second well region. Accordingly, applicants respectfully submit that claim 28 further distinguishes over AAPA, alone or in combination, with the Chen reference.

Claim 29 further distinguishes over the Chen reference and the AAPA. Claim 29 recites:

> The input protection circuit of claim 1, wherein the third and fourth well regions are not part of a MOS transistor.

The Chen reference does not teach, suggest, or disclose the input protection circuit of claim 1. Instead, the Chen reference discloses that the third and fourth well regions (36 and 34) are part of a MOS transistor. The MOS transistor is formed by a gate structure 37 that overlies a portion of the P-type semiconductor layer 30 between

the N-typed doped regions 34 and 36. (Chen, Col. 3, lines 28 - 37). Accordingly, applicants respectfully submit that claim 29 distinguishes over the Chen reference.

The AAPA does not make up for the deficiencies of the Chen reference. Assuming, *arguendo*, that n-type well regions 3 and 4 were the third and fourth well regions, which they are not, then these two n-type well regions (the third and fourth well regions) are part of a MOS transistor. This is completely opposite to claim 29, where the third and fourth well regions are not part of a MOS transistor. Accordingly, applicants respectfully submit that claim 29 distinguishes over the AAPA, alone or in combination with the Chen reference.

Independent claim 5 recites:

An input protection circuit comprising:

an input terminal for supplying an input signal to a circuit to be protected;

a semiconductor substrate of a first conductivity type;

a first well region of a second conductivity type opposite to the first conductivity type, said first well region being formed in one principal surface area of said semiconductor substrate and forming a PN junction with said semiconductor substrate;

first and second impurity doped regions of the first conductivity type formed in said first well region and forming a first lateral bipolar transistor with a portion of said first well region serving as a base;

second and third well regions of a second conductivity type formed in the principal surface area of said semiconductor substrate, said second and third well regions forming a second lateral bipolar transistor with a portion of said semiconductor substrate serving as a base;

a circuit formed in said semiconductor substrate and connected to said input terminal;

wherein said input terminal is connected to said first impurity doped region, ***said second impurity doped region and the base of said first lateral bipolar transistor are connected to said second well region***, said first lateral bipolar transistor operating without a fixed base bias, and said third well region and the base of the second lateral bipolar transistor are connected to one reference potential node.

The Groeseneken reference is related to a semiconductor device for electrostatic discharge or overvoltage protection. The Examiner states that the Groeseneken reference teaches in Fig. 5 an input protection circuit comprising: a semiconductor

substrate of a first conductivity type; a first well region 51 of a second conductivity type, the first well region being formed in one principal surface area of the semiconductor substrate forming a PN junction with the semiconductor substrate; first and second impurity doped regions 541, 542 of the first conductivity type formed in the first well region and forming a first bipolar transistor with a portion of the first well serving as a base; third and fourth regions 551, 552 of the second conductivity type formed in the semiconductor substrate and forming a second lateral bipolar transistor with a portion of the semiconductor substrate serving as a base. *(July 8 Office Action, pages 5 and 6)*.

The Groeseneken reference does not disclose, teach, or suggest the input protection circuit of claim 5. The Groeseneken reference does not concern an input protection circuit comprising: an input terminal for supplying an input signal to a circuit to be protected; a semiconductor substrate of a first conductivity type; a first well region of a second conductivity type opposite to the first conductivity type, said first well region being formed in one principal surface area of said semiconductor substrate and forming a PN junction with said semiconductor substrate; first and second impurity doped regions of the first conductivity type formed in said first well region and forming a first lateral bipolar transistor with a portion of said first well region serving as a base; **second and third well regions of a second conductivity type formed in the principal surface area of said semiconductor substrate**, said second and third well regions forming a second lateral bipolar transistor with a portion of said semiconductor substrate serving as a base; a circuit formed in said semiconductor substrate and connected to said input terminal; wherein said input terminal is connected to said first impurity doped region, **said second impurity doped region and the base of said first lateral bipolar transistor are connected to**

said second well region, said first lateral bipolar transistor operating without a fixed base bias, and said third well region and the base of the second lateral bipolar transistor are connected to one reference potential node.

As stated by the Examiner, the second and third regions in the Groeseneken reference (the Examiner lists third and fourth regions in his remarks but the claim recites second and third regions) are not taught as being second and third well regions. *(July 8 Office Action, page 6)*. Thus, the input protection circuit of the Groeseneken reference cannot include **second and third well regions of a second conductivity type formed in the principal surface area of said semiconductor substrate.** Accordingly, applicants respectfully submit that claim 5 distinguishes over the Groeseneken reference.

Claim 5 further distinguishes over the Groeseneken reference. The Groeseneken reference does not concern an input protection circuit wherein **said second impurity doped region and the base of said first lateral bipolar transistor are connected to said second well region.** Assuming, *arguendo*, that second region 551 is a second well region, the Groeseneken reference discloses that its second impurity doped region 542 is connected to the alleged second well region 551, but does not disclose that the N-well 51 is connected to the second well region 551. This is not the same as an input protection circuit **where the second impurity doped region and the base of said first lateral bipolar transistor are connected to said second well region.** Accordingly, applicants respectfully submit that claim 5 distinguishes over the Groeseneken reference.

The Chen reference does not make up for the deficiencies of the Groeseneken reference. Unlike the input protection circuit of claim 5, the Chen reference does not concern an input protection circuit including **second and third well regions of a second**

conductivity type formed in the principal surface area of said semiconductor substrate. The Examiner states that the Chen reference does not teach the third and fourth regions being well regions (the third and fourth regions of claim 1 correspond to the second and third well regions of claim 5). *(July 8th Office Action, page 4)*. Thus, the Chen reference does not disclose an input protection circuit including second and third well regions of a second conductivity type. Accordingly, applicants respectfully submit that claim 5 distinguishes over the Chen reference, alone or in combination, with the Groeseneken reference.

In addition, unlike the input protection circuit of claim 5, the Chen reference does not concern an input protection circuit wherein **said second impurity doped region and the base of said first lateral bipolar transistor are connected to said second well region.** Assuming, arguendo, that the Chen reference does have a second well region, the Chen reference only discloses that the base of a first bipolar transistor is connected to the second well region. There is no disclosure that the second impurity doped region is connected to said second well region, as is recited in independent claim 5. Accordingly, applicants respectfully submit that claim 5 distinguishes over the Chen reference, alone or in combination, with the Groeseneken reference.

The applicant admitted prior art (AAPA) does not make up for the deficiencies of the Groeseneken and Chen references. Unlike the input protection circuit of claim 5, the AAPA does not concern an input protection circuit wherein **said second impurity doped region and the base of said first lateral bipolar transistor are connected to said second well region.** Because the AAPA is not an input protection circuit including two bipolar transistors (where the second bipolar transistor is formed including the second well

region and the third well region) it is impossible for the AAPA to include a second well region as recited in independent claim 5. Accordingly, applicants respectfully submit that claim 5 further distinguishes over the AAPA, alone or in combination with the Chen and Groeseneken references.

The Watt reference does not make up for the deficiencies of the Chen reference and the AAPA. The Examiner states that the Watt reference teaches forming a resistor in on a semiconductor substrate. *(July 8 Office Action, page 8)*. Assuming, *arguendo*, that the Watt reference does disclose forming of a resistor in a semiconductor substrate, the Watt reference does not disclose an input protection circuit including ***second and third well regions of the second conductivity type formed in the principal surface area of said semiconductor substrate, and said second and third well regions forming a second lateral bipolar transistor with a portion of said semiconductor substrate serving as a base*** or an input protection circuit wherein **said second impurity doped region and the base of said first lateral bipolar transistor are connected to said third well region.** Accordingly, applicants respectfully submit that claim 5 distinguishes over the Watt reference, alone or in combination with the Groeseneken and Chen references and the AAPA.

Further, applicants respectfully submit that the Groeseneken reference and the AAPA cannot be combined because there is no teaching, suggestion, or incentive to support the combination of the Groeseneken reference and the AAPA. The Groeseneken reference does not disclose that its second and third regions (551 and 552) can be well regions, as supported by the Examiner's statement "Groesenken does not teach third or fourth regions being third and fourth well regions." *(July 8, 2003 Office Action, page 6)*.

The AAPA does not mention the utilization of six impurity doped regions and two transistors to form an input protection circuit, as the Groeseneken reference does. By combining these references, the Examiner has impermissibly used "hindsight" by using the applicant's teaching as a blueprint to hunt through the prior art for the claimed elements and then combine them as claimed. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991).

In addition, the combination of the Groeseneken reference with the AAPA reference would destroy the purpose and intent of the invention disclosed in the Groeseneken reference. This would be a disincentive for combining the references. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984). AAPA discloses an n-channel MOS transistor FT which includes a drain (well region 3), a gate (electrode layer 9), and a source (well region 4). The AAPA also discloses a bipolar transistor BT made of well regions 3 and 4 and a p-type region (portion of the well region 2). Placing the AAPA's circuit into the Groesenken reference's circuit would destroy the purpose of the Groeseneken refeerence because the Groeseneken reference either utilizes MOS transistors or parasitic bipolar transistors to establish a protection circuit (Groeseneken reference Figs 5 and 6). It does not disclose the utilization of both MOS and bipolar transistors together within the same circuit, as is disclosed by the AAPA. The production of the Groeseneken circuit would have to be completely revamped to include the formation of a MOS transistors with the bipolar transistors. Thus, the Groeseneken and AAPA cannot properly be combined.

Claims 6, 25, and 26, depend directly from claim 5. Accordingly, applicants respectfully submit that claims 6, 25 and 26 distinguish over the Groeseneken, Chen,

AAPA, and Watt references, alone or in combination, for the same reasons as discussed above in regard to independent claim 5.

Independent claim 9 recites:

> A semiconductor input protection circuit comprising:
>
> a semiconductor substrate;
>
> a first active region of a first conductivity type defined in said semiconductor substrate;
>
> a second active region of a second conductivity type defined in said semiconductor substrate;
>
> first and second impurity doped regions of the second conductivity type formed in said first active region;
>
> third and fourth impurity doped regions of the first conductivity type formed in said second active region;
>
> an input terminal connected to said first impurity doped region;
>
> a first wiring for connecting said first active region and said second impurity doped region to said third impurity doped region; and
>
> **a second wiring for connecting only said second active region and said fourth impurity doped region to a reference potential.**

The Bhatia reference is directed towards a field effect transistor structure which eliminates the problems caused by parasitic currents between devices within the structure, i.e., it does not provide input protection for a signal. The Examiner states that Bhatia teaches a semiconductor substrate 2, a first active region 4 of a first conductivity type defined in the semiconductor substrate, a second active region 6 of a second conductivity type defined in the semiconductor substrate, first and second impurity doped regions 22 and 20 of the second conductivity type formed in the first active region; third and fourth impurity doped regions 15, and 18 of the first conductivity type formed in the second active region; a terminal +VH connected to the first impurity doped region; a first wiring for connecting the first active region and the second impurity

doped region 20 to the third impurity dope region 15; and a second wiring for connecting the second active region and the fourth impurity doped region 18 to a reference potential. *(July 8 Office Action, page 9)*. The second wiring is also connected to a guard region, i.e., 15, located in the active region 6. *(Bhatia, Fig. 3, col. 4, lines 58 – 61)*.

The Bhatia reference does not disclose, teach, or suggest the semiconductor input protection circuit of claim 9, as amended. The Bhatia reference does not concern a semiconductor input protection circuit including a semiconductor substrate; a first active region of a first conductivity type defined in said semiconductor substrate; a second active region of a second conductivity type defined in said semiconductor substrate; first and second impurity doped regions of the second conductivity type formed in said first active region; third and fourth impurity doped regions of the first conductivity type formed in said second active region; an input terminal connected to said first impurity doped region; a first wiring for connecting said first active region and said second impurity doped region to said third impurity doped region; and **a second wiring for connecting only said second active region and said fourth impurity doped region to a reference potential**.

Instead, the Bhatia reference discloses utilizing a wiring to connect the second active region, a fourth impurity doped region 20, and a region 15 in the first active region 6 to ground potential. This is not the same as connecting **only said second active region and said fourth impurity doped region** because the Bhatia reference includes the extra connection to region 15 in the first active region 6. Accordingly, applicants respectfully submit that claim 9 distinguishes over the Bhatia reference.

AAPA does not make up for the deficiencies of the Bhatia reference. AAPA is directed to an input protection circuit which includes only one active region, the p-well 2, and two well regions 3 and 4, inside the p-well 2. There are three impurity doped regions disclosed, i.e., regions 5, 6, and 7, but no fourth impurity doped region is disclosed. Thus, it is impossible for the AAPA to have a second wiring for connecting only said second active region and said fourth impurity doped region to a reference potential, as recited in claim 9, because the AAPA has no fourth impurity doped region. Accordingly, applicants respectfully submit that claim 9, as amended, distinguishes over the AAPA, alone or in combination with the Bhatia reference.

The Iwase reference does not make up for the deficiencies of the Bhatia reference. The Iwase reference discloses a first wire connecting an input terminal 13, a p-type impurity doped region 18 (a first impurity doped region) in a first active region 16, a n-type impurity doped region 24 in a second active region 22 and a high-potential power supply and a low-potential power supply. The Iwase reference also discloses a wire connecting a p-type impurity doped region 17 (second impurity doped region) in a first active region 16, a n-type impurity doped region 23 (third impurity doped region) in a second active region 22, and ground potential Vss. The second active region 22 is also connected to a fixed voltage Vbb. *(Iwase, Fig. 3)*

The Iwase reference does not teach, suggest, or disclose the semiconductor input protection circuit of claim 9, as amended. Neither of the wirings disclosed in the Iwase reference connect only the second active region and the fourth impurity doped region to a ground potential. In the Iwase semiconductor device, the fourth impurity doped region is connected to the first impurity doped region in the first active region and a high-potential

power supply and a low-potential power supply. It is not the same as the semiconductor input protection circuit of claim 9 because the Iwase reference's wire is connected to a low potential and a high potential power supply and not a reference potential. Accordingly, applicants respectfully submit that claim 9, as amended, distinguishes over the Iwase reference, alone or in combination with the Bhatia reference and the AAPA.

The Watt reference does not make up for the deficiencies of the Bhatia reference, the AAPA, and the Iwase reference. The Watt reference discloses an ESD protection structure for p-well technology. In the Watt reference, three impurity doped regions could be the third and fourth impurity doped regions, which means that 57e or 57b could be the fourth well region. A wire connects 57e to the pad and the local ESD and input buffer. Another wire connects 57a, gate 57c, 57b, gate 57D, the p-well (via 57f), and a p-type impurity doped region to a metal conduit Vss 39.

The Watt reference does not disclose, teach, or suggest the semiconductor input protection circuit of claim 9, as amended. Regardless of whether 57e or 57b are the fourth well region, neither of the wirings in the Watt reference connect **only said second active region and said fourth impurity doped region to a reference potential** because 57e is connected only to the input pad, and 57 b is connected to a number of gates and other impurity doped regions. Accordingly, applicants respectfully submit that claim 9, as amended, distinguishes over the Bhatia reference, the AAPA, the Iwase reference and the Watt reference.

Further, applicants respectfully submit that the Bhatia reference, the AAPA, the Iwase, and the Watt references cannot be combined because there is no teaching, suggestion, or incentive to support their combination. By combining these references,

the Examiner has impermissibly used "hindsight" by using the applicant's teaching as a blueprint to hunt through the prior art for the claimed elements and then combine them as claimed. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991). First, the Bhatia reference is directed to a field effect transistor structure which eliminates the problems cause by parasitic current between devices. The other three references are directed to ESD protection structures for semiconductors. One would not look to the field of ESD protection structures to look for solutions in eliminating problems caused by parasitic current.

In addition, each of the references has a unique configuration of p- and n-type well regions, and n- and p-type impurity doped regions. For example, the Bhatia reference has a n-well (with one n-type doped region and three p-type doped regions) and a p-well (with three n-type doped regions and one p-type doped regions) while the Watt reference has two p-wells in an n-substrate, where one p-well has one p-type doped region and one n-type doped region and the other p-well has three n-type doped regions and one p-type doped region. The other two references also have different structures. The Examiner is utilizing pieces of incompatible structures in order to piece together the limitations of the applicant's claims. Thus, applicants respectfully submit that the Bhatia, Iwase, and Watt references and the AAPA are not properly combinable.

Claims 10, 12, and 14 – 19, depend, directly or indirectly on independent claim 9, as amended. Accordingly, applicants respectfully submit that claims 10, 12, and 14 – 19, all distinguish over the Bhatia reference, the AAPA, the Iwase reference, and the Watt reference, alone or in combination, for the same reasons as discussed above in regard to independent claim 9, as amended.

Applicants believe that the foregoing amendments place the application in condition for allowance, and a favorable action is respectfully requested. If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call either of the undersigned attorneys at the Los Angeles telephone number (213) 488-7100 to discuss the steps necessary for placing the application in condition for allowance should the Examiner believe that such a telephone conference would advance prosecution of the application.

Respectfully submitted,

PILLSBURY WINTHROP LLP

Date: January 8, 2004

By: _____
Mark R. Kendrick
Registration No. 48,468
Attorney for Applicant(s)

Date: January 8, 2004

By: _____
Roger R. Wise
Registration No. 31,204
Attorney For Applicant(s)

725 South Figueroa Street, Suite 2800
Los Angeles, CA 90017-5406
Telephone: (213) 488-7100
Facsimile: (213) 629-1033